UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,167	12/02/2008	**Ralf Wirth**	12406-212US1 P2004,0150 U	5063

26181 7590 03/21/2012
FISH & RICHARDSON P.C. (SV)
PO BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
WOLDEGEORGIS, ERMIAS T	
ART UNIT	**PAPER NUMBER**
2893	

NOTIFICATION DATE	DELIVERY MODE
03/21/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/588,167	WIRTH ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) *21-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 59* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/27/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *WO03044872*.

DETAILED ACTION

1. ***Response to Amendment***

Claims 1, 2 and 17 have been amended; claims 21-58 have been withdrawn; and claims 1-59 are currently pending.

2. ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

3. ***Information Disclosure Statement***

The information disclosure statement filed on 12/27/2011 has been acknowledged and a signed copy of the PTO-1449 is attached herein.

4. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 13-16, 20 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno et al. **(WO 03044872, hereinafter "Kohno"; its US equivalent PG. Pub.**

2005/0012109 A1 is used for rejection) in view of Ishikawa et al. **(USPN 5977565, hereinafter "Ishikawa")**

In regards to claim 1, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) an optoelectronic component comprising a semiconductor function region **(14+15+16)** with an active zone **(15)** and a lateral main direction of extension **(D100)**, wherein said semiconductor function region **(14+15+16)** is provided with at least one opening **(10)** through said active zone **(15)** in a direction orthogonal to the main direction **(D100)**, and disposed in the region of said opening **(10)** is a connecting conductor material **(31)** that is electrically isolated from said active zone **(15)** at least in a subregion of said opening.

However, Kohno fails to explicitly teach that the connecting conductor material extends entirely through said active zone.

Ishikawa while disclosing a semiconductor light emitting diode (abstract) teaches (Fig. 8) the connecting conductor material **(105)** extends entirely through said active zone **(103)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a connecting conductor material extending through entire active zone because, as taught by Ishikawa in col. 1 lines 34-53, having the structural arrangement of Ishikawa would create a capacitor between electrodes, and/or between electrode and semiconductor layers that would improve reliability of the device by avoiding the

deterioration of characteristics such as lowering of a luminous efficiency when a high voltage is applied. As a result, the handling of the device would be easier without deterioration when a voltage surge takes place.

In regards to claim 2, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) an optoelectronic component comprising a semiconductor function region **(14+15+16)** with an active zone **(15)** and a lateral main direction of extension **(D100)**, wherein said semiconductor function region **(14+15+16)** is provided with a lateral side face **(100)** bounding said active zone **(15)**, and disposed after said side face**(100)** in the lateral direction is a connecting conductor material **(31)** that is electrically isolated from said active zone **(15)** at least in a subregion of said side face **(100)**.

However, Kohno fails to explicitly teach that the connecting conductor material extends over an entire length of said active zone in a direction orthogonal to the main direction.

Ishikawa while disclosing a semiconductor light emitting diode (abstract) teaches (Fig. 8) the connecting conductor material **(105)** extends over an entire length of said active zone **(103)** in a direction orthogonal to the main direction **(direction parallel to the substrate)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a connecting conductor material extending through entire active zone because, as taught by Ishikawa in col. 1 lines 34-53, having the structural

arrangement of Ishikawa would create a capacitor between electrodes, and/or between electrode and semiconductor layers that would improve reliability of the device by avoiding the deterioration of characteristics such as lowering of a luminous efficiency when a high voltage is applied. As a result, the handling of the device would be easier without deterioration when a voltage surge takes place.

In regards to claim 3, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material **(31)** is at least partially electrically isolated from said active zone **(15)** by an isolation material **(102)**.

In regards to claim 4, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening **(10)** is configured as a depression in the lateral direction **(D100)** or said side face **(100)** is provided with a depression in the lateral direction **(D100)**.

In regards to claim 5, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said isolation material **(102)** at least partially lines said opening **(10+2).**

In regards to claim 6, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening **(10)** extends in the vertical direction **(D200)** all the way through said semiconductor function region **(14+15+16)**.

In regards to claim 7, Kohno as modified by Ishikawa discloses (see Fig. 8, Ishikawa) said semiconductor function region **(14+15+16)** comprises a first main face **(99)** and a second main face **(99')** located oppositely from said first main face **(99)** relative to said active zone **(15)**, and said semiconductor function region **(14+15+16)** is connected electrically conductively to said connecting conductor material **(31)** on the side comprising said first main face **(99)**.

In regards to claim 8, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material **(31)** is electrically isolated from said second main face **(99')** of said semiconductor function region **(14+15+16)**.

In regards to claim 9, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening **(10)** but fails to explicitly teach that the lateral dimension of said opening is equal to 100 μm, or less.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725

F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Finally, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the lateral dimension of the opening 100μm or less since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. ***In re Aller, 105 USPQ 233.***

In regards to claim 13, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said semiconductor function region **(14+15+16)** is disposed on a carrier **(11)**.

In regards to claim 14, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material **(31)** extends to a side of said carrier **(11)** that is opposite said semiconductor function region **(14+15+16)**.

In regards to claim 15, Kohno discloses **(Par [0071])** said component **(1)** can be fabricated in the wafer composite.

In regards to claim 16, Kohno discloses **(Par [0071])** said semiconductor function regions **(14+15+16)** are disposed at least partially side by side in the lateral direction.

In regards to claim 20, Kohno discloses **(Par [0071])** said device **(1)** can be fabricated in the wafer composite.

In regards to claim 59, Kohno as modified by Ishikawa discloses said isolation material **(102)** is disposed at least partially on said side face **(100).**

6. Claims 10-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno in view of Ishikawa as applied to claim 1 or 2 above; and further in view of Oshio et al. **(US 2001/0042865 A1, hereinafter "Oshio")**.

In regards to claims 10 and 11, Kohno as modified by Ishikawa discloses all limitations of claim 1 or 2 above but fails to explicitly teach an envelope forms at least partially around said semiconductor function region (claim 10); and said envelope is transparent to a radiation to be generated or received by said active zone (claim 11).

Oshio while disclosing a semiconductor light emitting device (abstract) teaches (Fig. 1) an envelope **(5)** forms at least partially around said semiconductor function region **(1)** (claim 10); said envelope **(5)** is transparent **(Par [0046])** to a radiation to be generated or received by said active zone **(1)**(claim 11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno as modified by Ishikawa because, as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking. Furthermore, according to Oshio Par [0070], having the encapsulation would converge the light emitted from the light emitting element to improve the luminance remarkably.

In regards to claim 12, Kohno as modified by Ishikawa discloses all limitations of claim 1 or 2 above but fails to explicitly teach said active zone is surrounded by an encapsulation that is substantially hermetically tight.

Oshio discloses (Fig. 1) said active zone **(1)** is surrounded by an encapsulation **(9)** that is substantially hermetically tight.

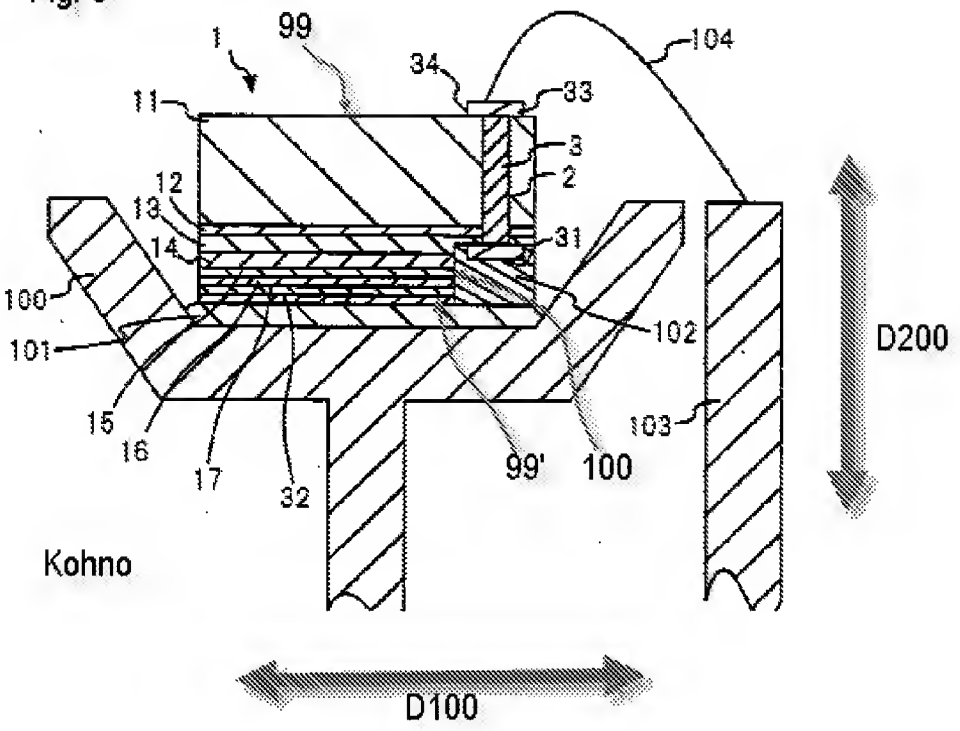
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno as modified by Ishikawa because as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking. Furthermore, according to Oshio Par [0070], having the encapsulation would help converge the light emitted from the light emitting element to improve the luminance remarkably.

In regards to claims 17-19, Kohno as modified by Ishikawa discloses all limitations of claim 16 above but fails to explicitly teach an envelope forms at least partially around said semiconductor function region, and said envelope is configured in one piece and at least partially forms around said semiconductor function regions (claim 17); said semiconductor function regions are mechanically stabilized by a stabilization layer (claim 18); and said envelope is configured as a stabilization layer or part of said stabilization layer (claim 19).

Oshio discloses (Fig. 1) said envelope **(5)** is configured in one piece and at least partially forms around said semiconductor function regions **(1);** said semiconductor function regions **(1)** are mechanically stabilized by a stabilization layer **(5+10A)**; and said envelope **(5)** is configured as a stabilization layer or part of said stabilization layer **(5+10A)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno as modified by Ishikawa because as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking.

Fig. 3



7. ***Response to Arguments***

Applicant's arguments with respect to claims 1 and 2 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

8. ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893

/Matthew Reames/
Primary Examiner, Art Unit 2893